This project has received funding from the European Union's Horizon 2020 research and innovation programme

High Density 3D CMOS Mixed-Signal Opportunities

The **3D-MUSE** project

Univ. of Oslo, CEA/LETI, IDEAS AS, Lund University, ST Microelectronics, INP Grenoble

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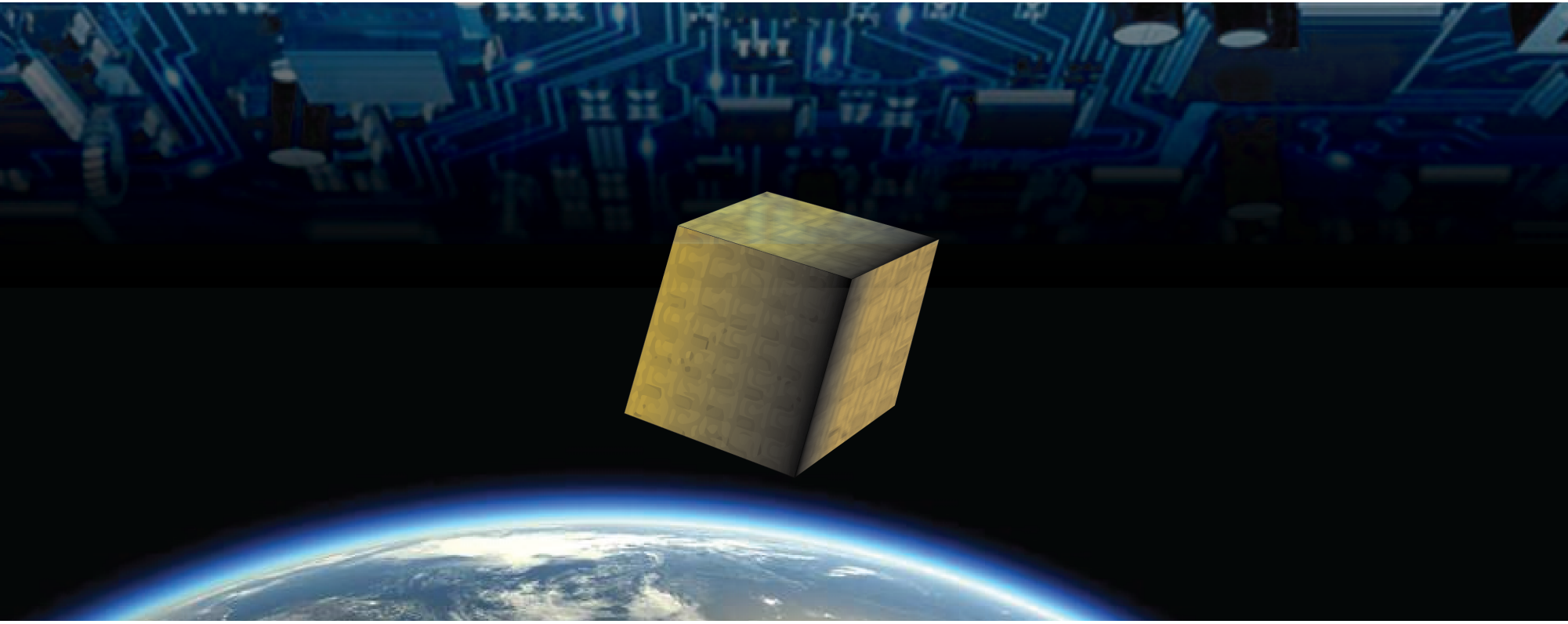
3D-MUSE



System-in-Cube (SinC) Smart Sensor Interfaces (SSI)
in Sequential 3D CMOS Technology

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Bottlenecks for IoT/portable devices

More challenging to scale (power, size, price) than digital electronics:

- mixed signal circuits
- sensors
- communication (antennas)
- energy supply

Conclusion:

- Digital electronics is no longer the bottleneck for the IoT.
- The main sales argument for IoT devices is not more processing power/memory
- The main sales argument for IoT devices is the number of ways they can interact with the real world

Bottlenecks for IoT/portable devices

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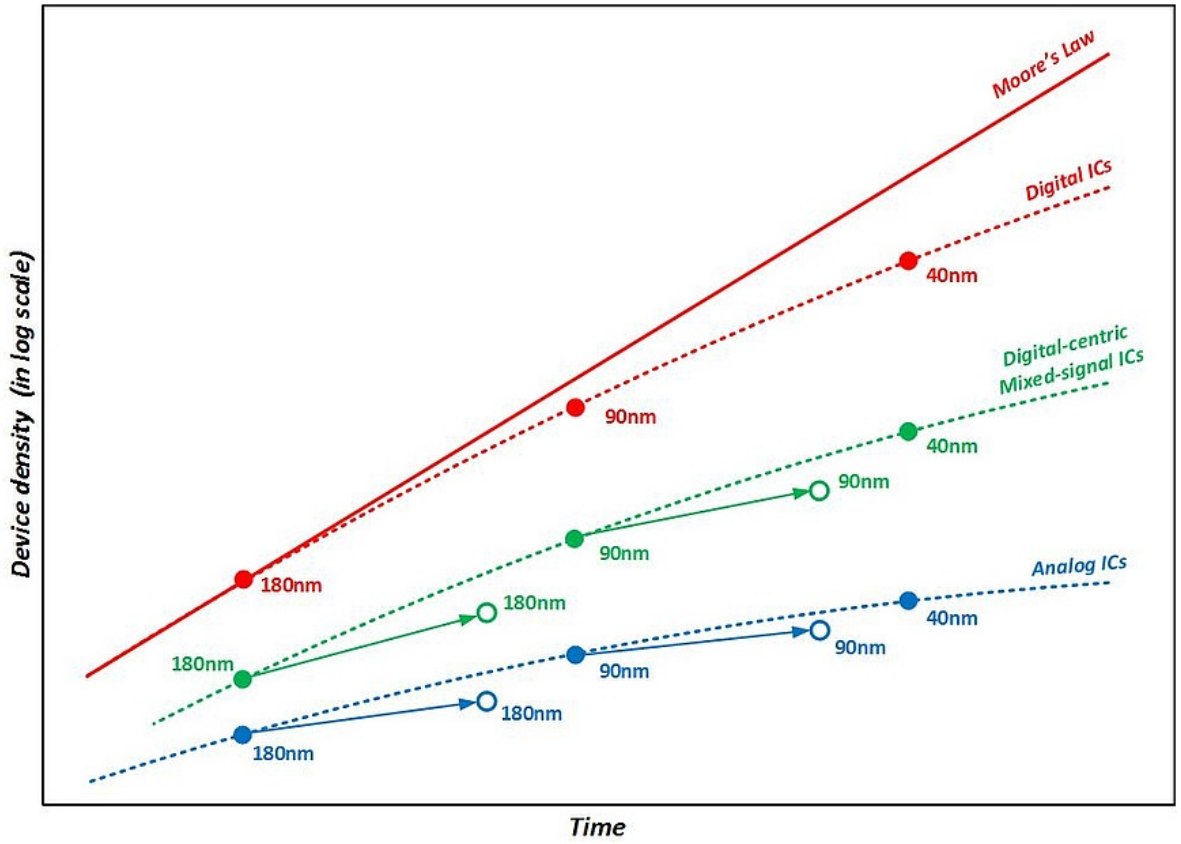
Analog and Mixed-Signal do not scale according to Moore's Law



courtesy of SiLabs

`http://www.embedded-computing.com/processing/`

`the-art-and-science-of-rf-and-mixed-signal-design`

Consequence:
While the price per digital device is going down with more adavaned CMOS technology, the price per analog device is actually going up.

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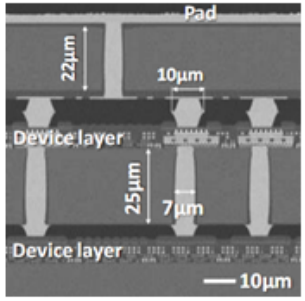
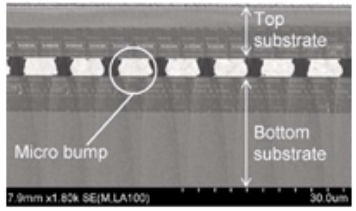
Parallel 3D integration

Trans-Silicon Via (TSV) pitch still above 1-2μm

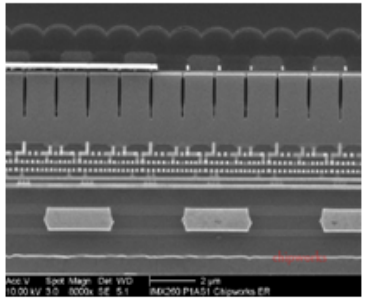
Industrial



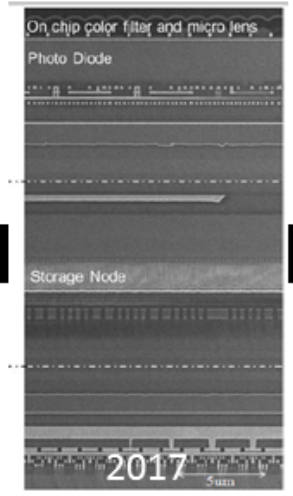
20 µm pitch Cu-PBO hybrid bonding (Hitachi)



10 µm pitch micro-bumps stacking (Olympus)



6 µm pitch Cu-SiO_2 hybrid bonding (Sony)

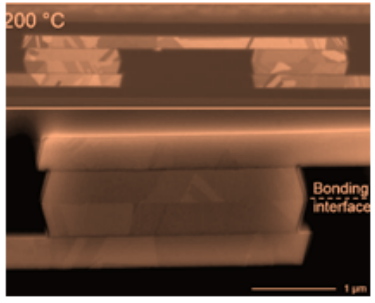


3 layers stack (BSI/Logic/DRAM) – (ISSCC Sony)

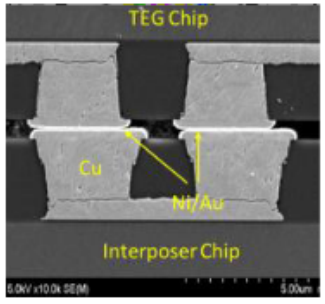
2014 2015 2016

Academic

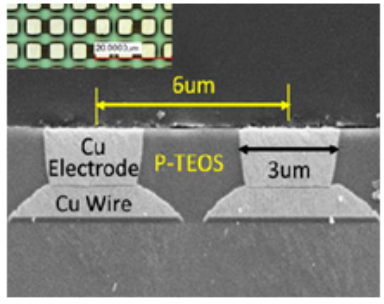
7 µm pitch Cu/SiO_2 hybrid bonding (CEA-Leti)



6 µm pitch Cu bonding with Ni/Sn capping (Tohoku University)



6 µm pitch hybrid bonding Cu nano-pillars (Tohoku University)



→ No integration in the range of pixel pitch (1-2 µm)
→ Very first 3-Layers prototypes released early 2017

courtesy of CEA/LETI, Grenoble, France

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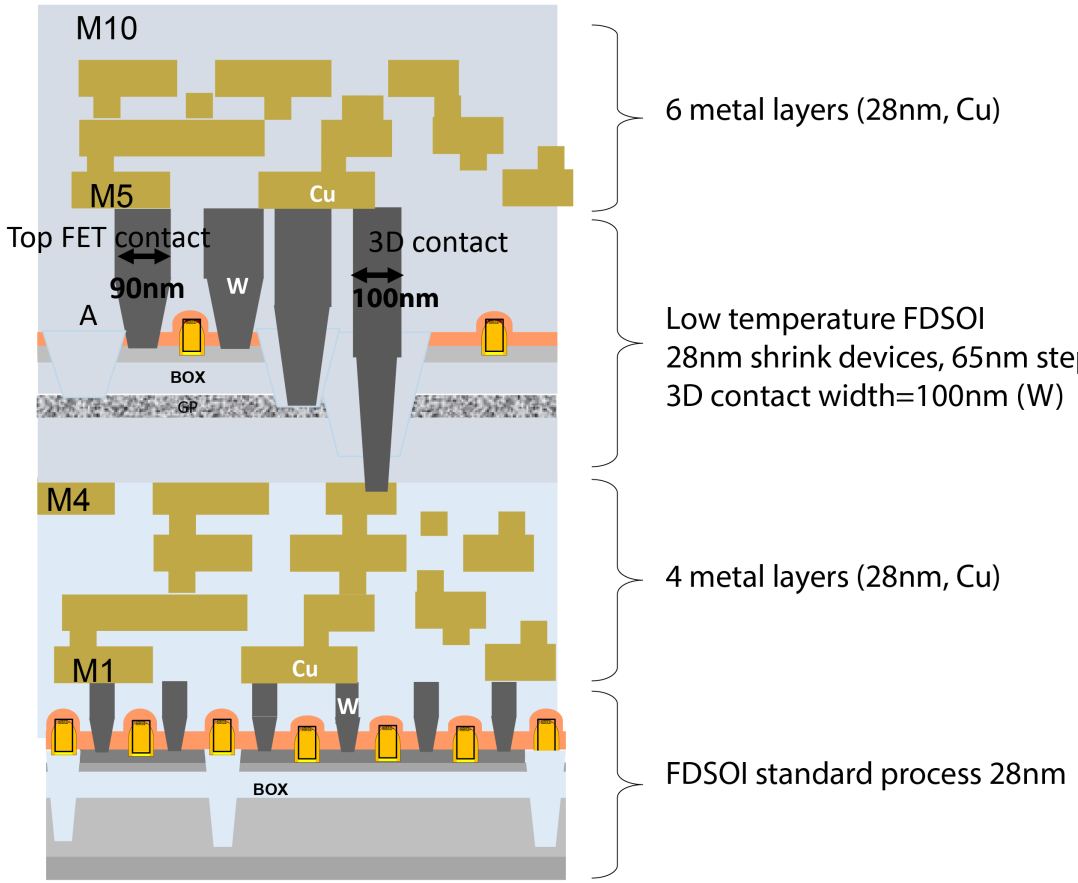
Sequential 3D integration (1/2)

Inter-Tier Interconnect pitch at 220nm (2017)

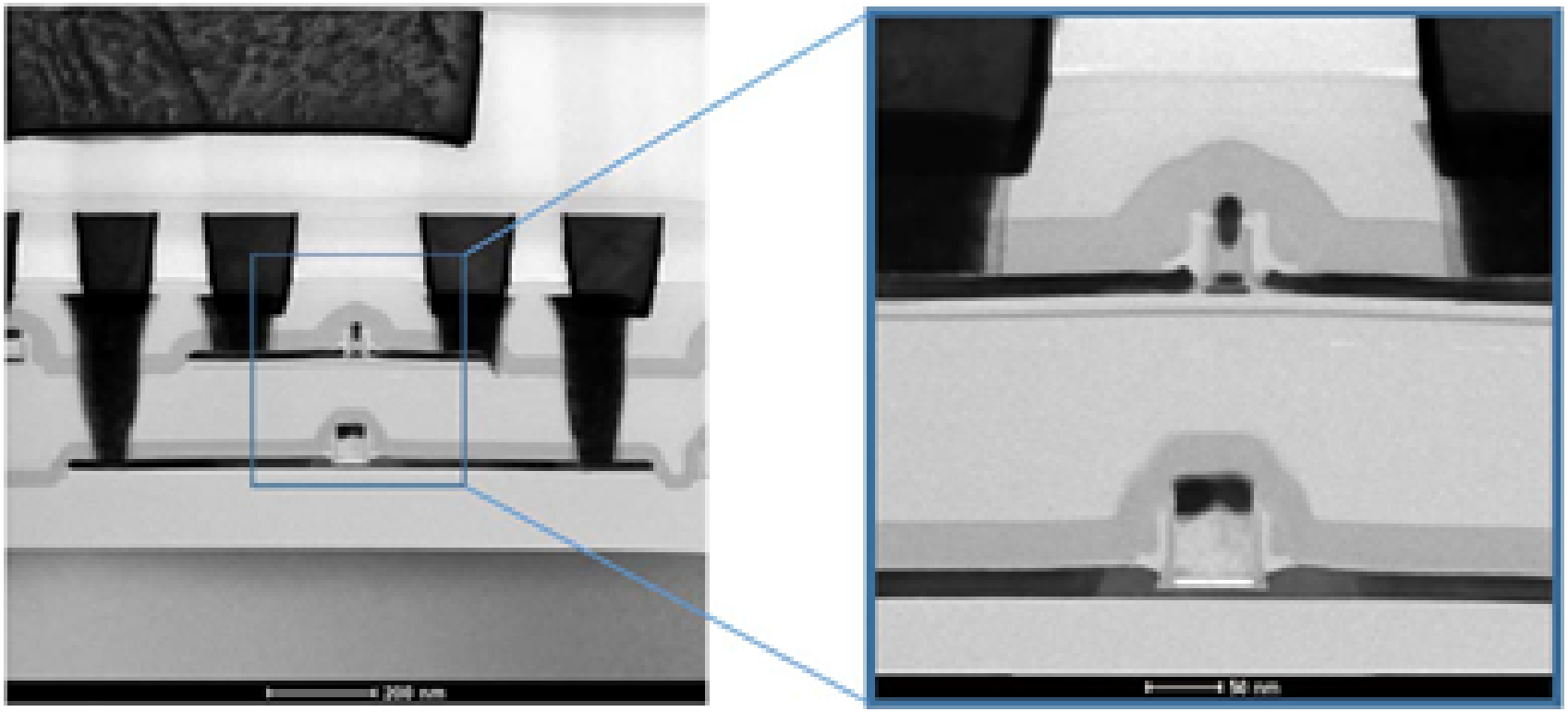
5-10x better than SoA, i.e. 25-100x better density

Unique to 3D-MUSE: inter-tier metal.



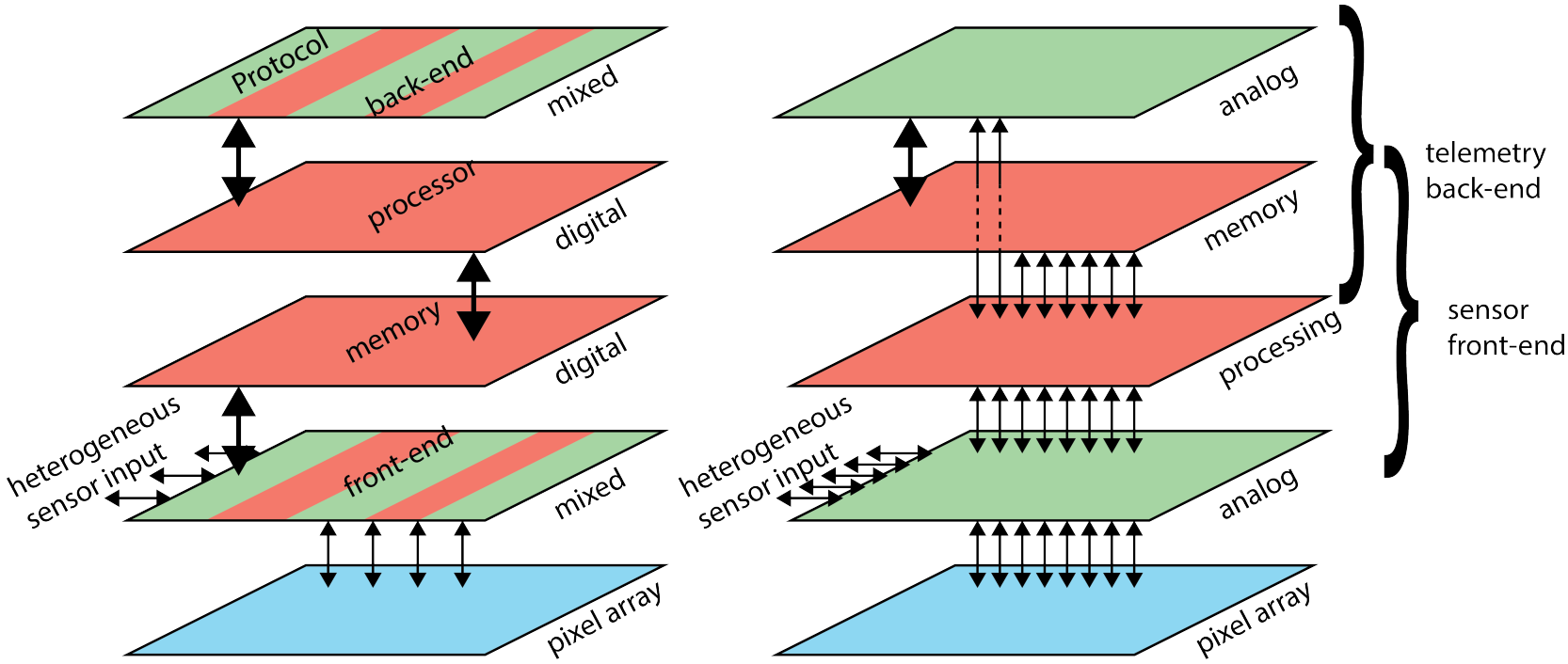
courtesy of CEA/LETI, Grenoble, France

Sequential 3D integration (2/2)



courtesy of CEA/LETI, Grenoble, France

System-in-Cube vs System-in-Stack



Adavantages in production cost, energy consumption, noise reduction, processing speed

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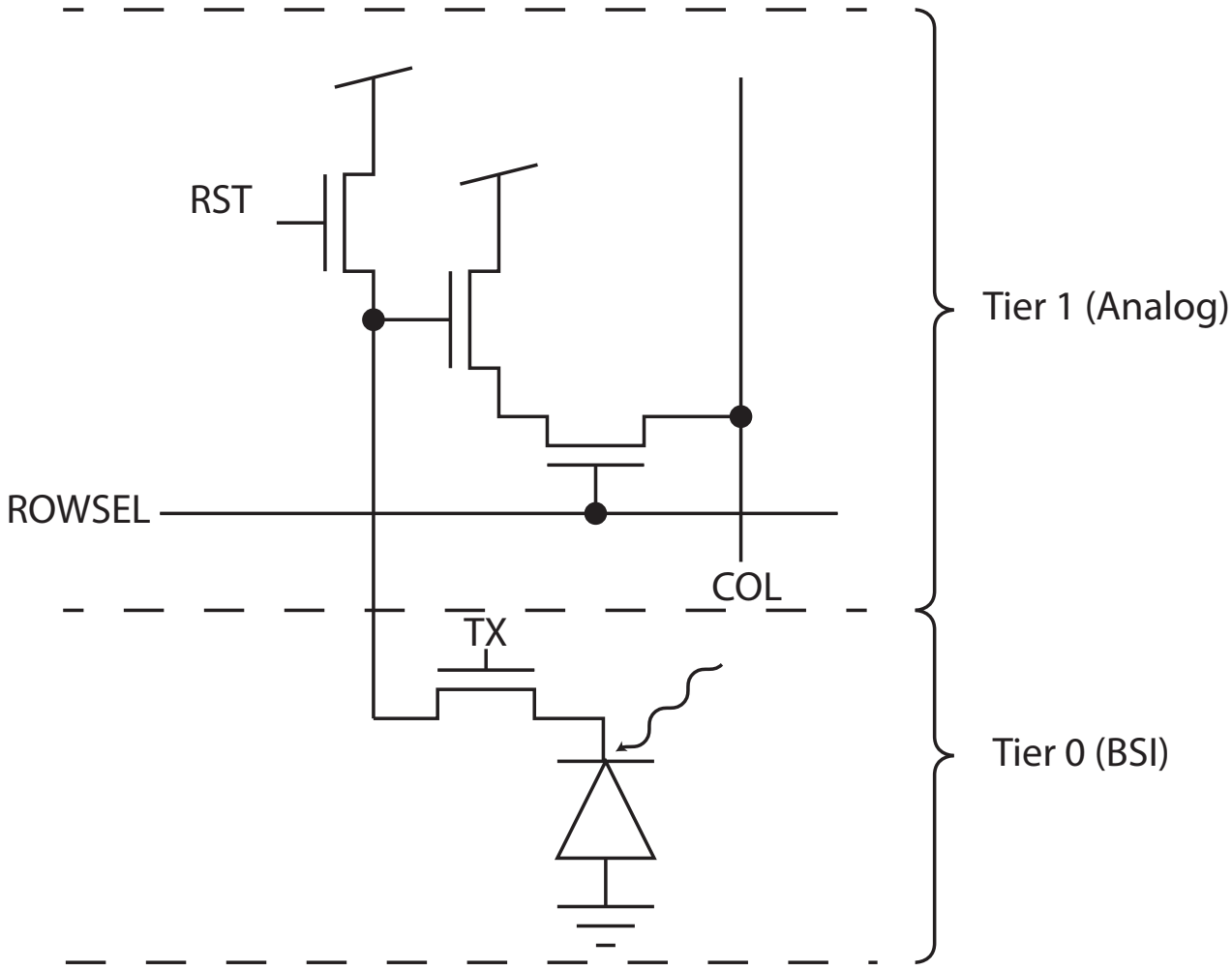
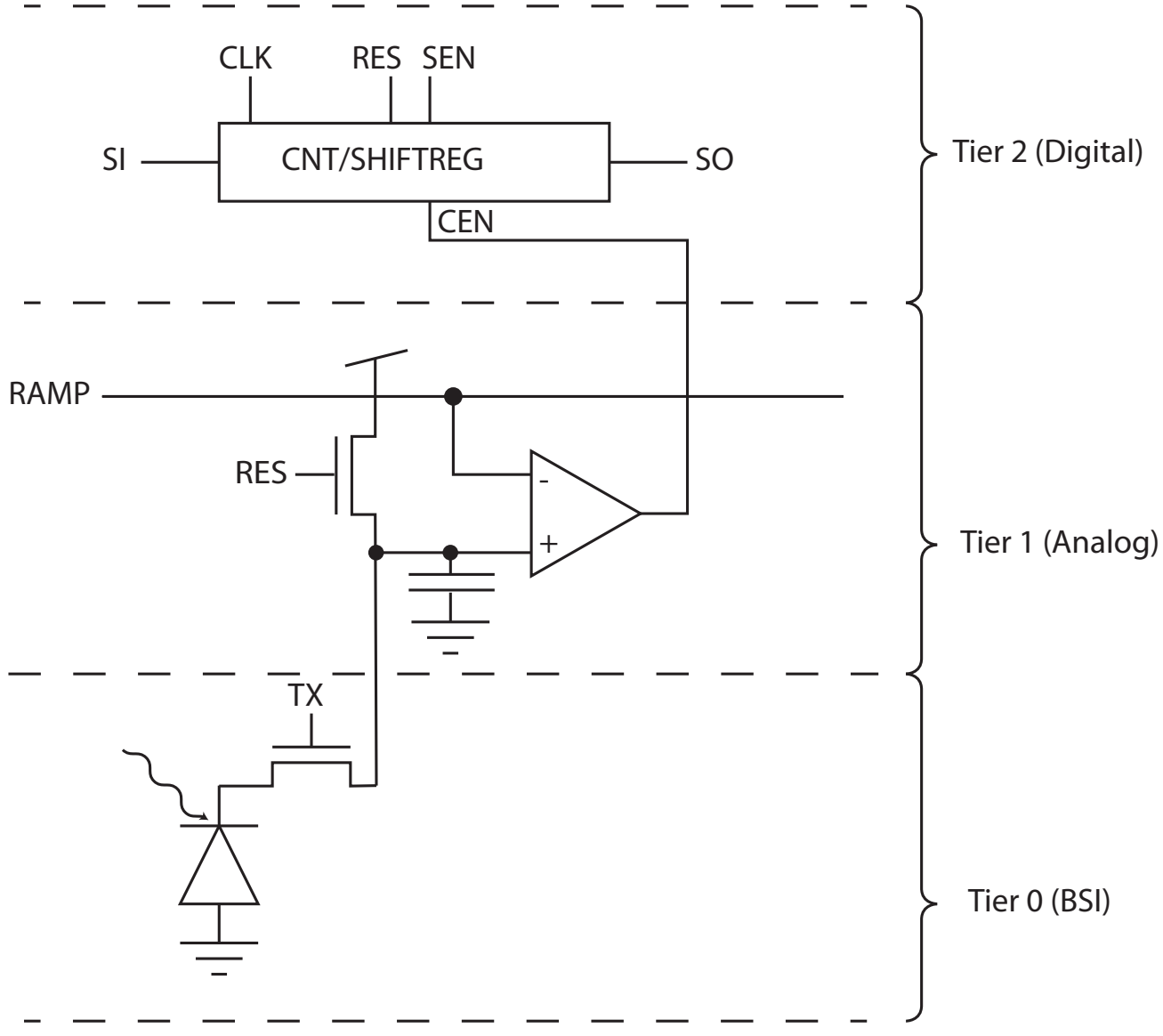
3D: BSI and APS

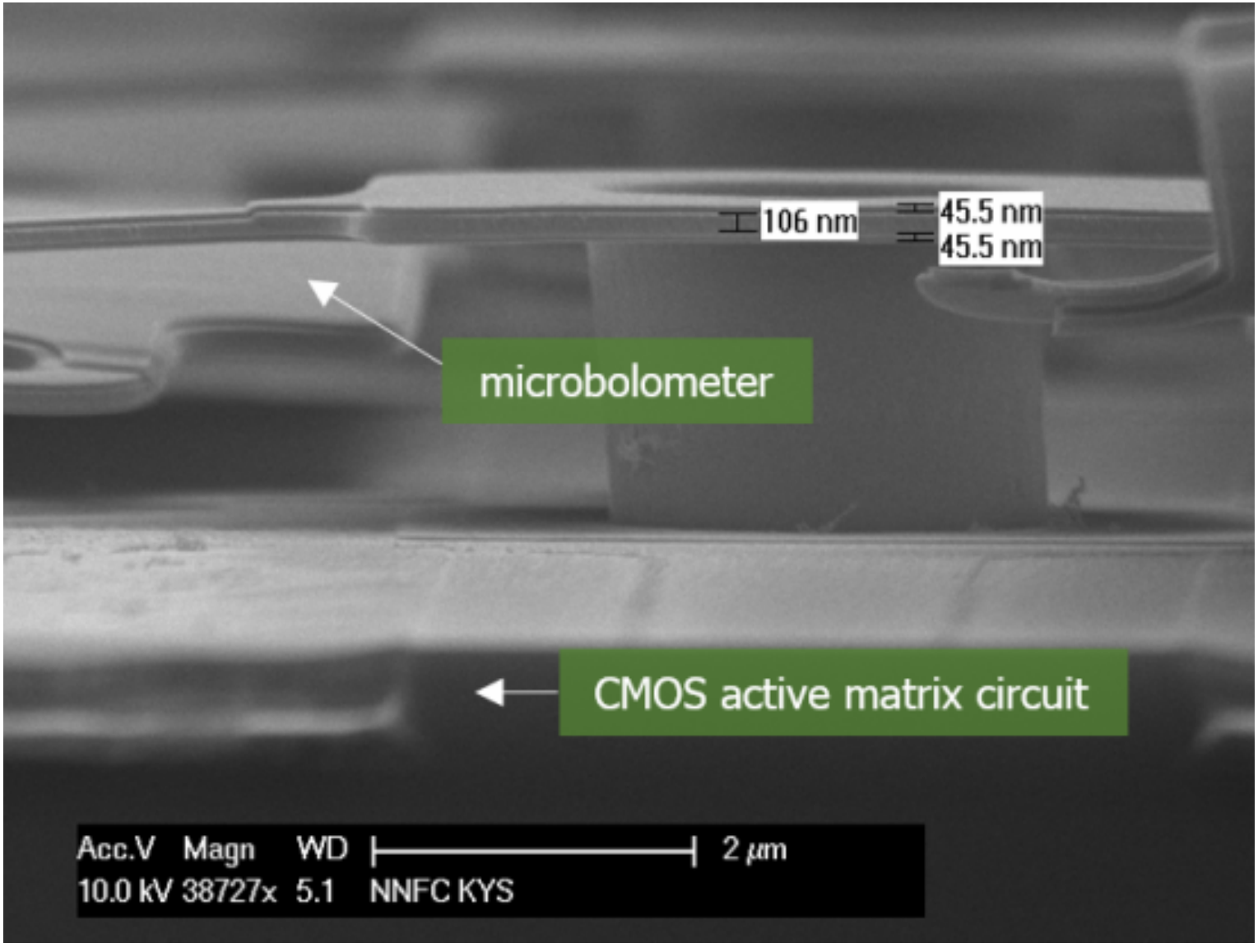
Even closer to 100% fill factor without micro-lens array. 'TSV' in the order of 100nm. Sub-$0.8^2 \mu m^2$ pixels?



3D: BSI and in-pixel ADC

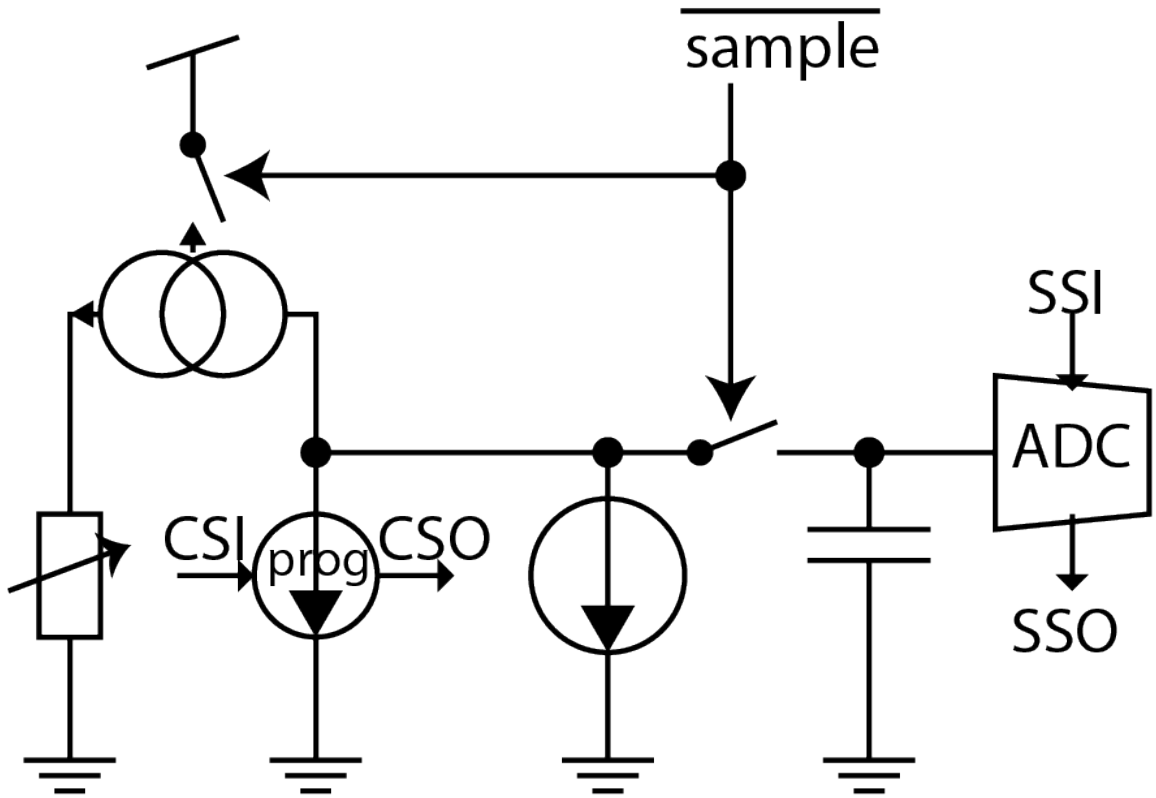


Micro-Bolometer Arrays



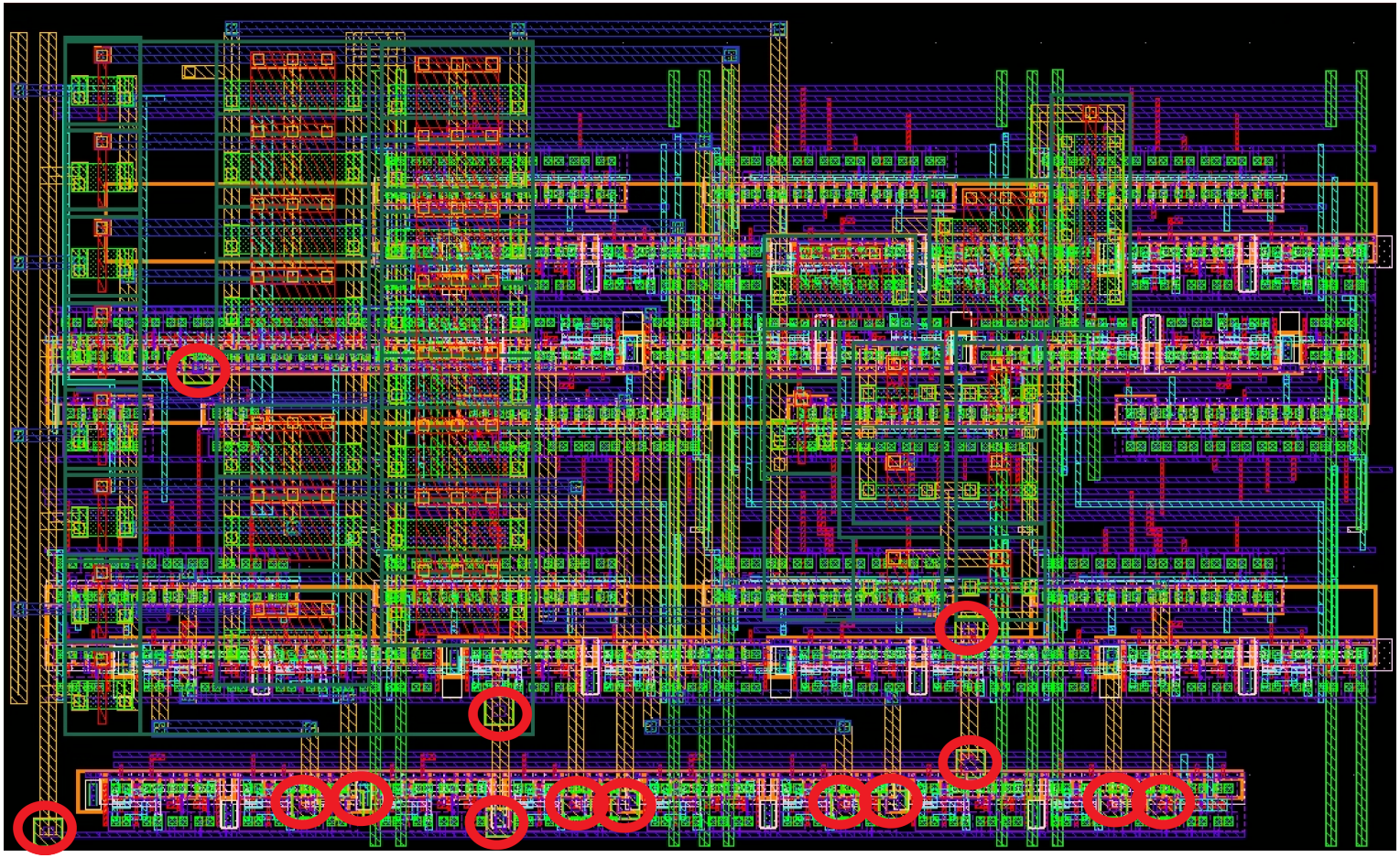
from 'Electro-Thermal Modeling and Experimental Validation of Integrated Microbolometer with ROIC' by Gyungtae Kim etal.

MBA ROIC Pixel 3DSI Block Diagram



Bolomter ROIC pixel concept: all 'analog' transistors in 65nm top tier all digital in 28nm bottom tier.

MBA ROIC Pixel 3DSI Layout



A 8μm $\times$ 13μm layout of a micro-bolometer array (MBA) 3DSI read-out integrated circuit (ROIC) pixel, FE, 10b ADC, 4b FPN calibration. 14 3D vias: 5 power, 8 calibration bits, 1 comparator output. Connection to MEMS bolometer would be parallel 3D, e.g. Cu-Cu.

3D: In general SIMD in a 2D array

(The Neuromorphs have done this for ages in 2D tech with abominable fill-factor)
Processing both in analog or digital domain. For example 2D-convolution (aka: feature maps, CNN, ...), image overlay, or even small general purpose in-pixel processors

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Take Home Messages

What I told you:

- digital is no longer the scaling bottleneck ...
- ... nor is it the most important sales argument
- e.g. mixed-signal is more challenging to scale, promising better pay off
- multi-process 3DSI is a mixed-signal designer's dream
- real circuits in a volume within reach with many benefits in cost and performance

What's next?

- near future developments will probably see a mix of monolithic/sequential and parallel 3D
- appropriate design tools are needed

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