2021 Nordic Circuits and Systems Conference (NorCAS)

VIRTUAL (Oslo, Norway) 26.-27.10.2021

Agenda (times in CEST = UTC+2!)

Tuesday Oct. 26

12:00 Opening (Chairs: Jari Nurmi, TAU, FI and Dag Wisland, Univ. Oslo, NO)

12:20 Keynote 1 (Chair: Jari Nurmi, TAU, FI)
Marja Matinmikko-Blue, University of Oulu, FI
6G Driving Sustainable Development

13:20 *Parallel sessions*

Session: Analog Circuits (Chair: Kristian Kjelgård, Univ. of Oslo, NO)

13:20 A 7.2µW Magnitude/Phase Bio-impedance Measurement Front-End with PWM Output in 0.18µm CMOS
Milad Zamani[1], Yasser Rezaeiyan[1], Omid Shoaei[2], Farshad Moradi[1]
1) Aarhus university, Denmark; 2) University of Tehran, Iran

13:40 A Two-Stage Single-Ended OTA with Improved Composite Transistors
Luis Henrique Rodovalho[1], Cesar Ramos Rodrigues[1], Orazio Aiello[2]
1) Federal University of Santa Catarina, Brazil;
2) National University of Singapore, Singapore

14:00 A 0.8-V, 2.88-GHz Double-Tail Latched Comparator in 22-nm FDSOI CMOS Technology
Harshitha Basavaraju[1,2], David Borggreve[1,2], Enno Böhme[1], Frank Vanselow[1], Erkan Nevzat Isa[1], Linus Maurer[1,2]
1) Fraunhofer EMFT, Munich, Germany;
2) Universität der Bundeswehr München, Neubiberg, Germany

Session: FPGAs and Accelerators (Chair: Peeter Ellervee, Tallinn Univ. of Tech., EE)

13:20 High-level Synthesis Implementation of an Accurate HEVC Interpolation Filter on an FPGA
Panu Sjövall, Matti Rasinen, Ari Lemmetti, Jarno Vanne; Tampere University, Finland

13:40 Unified OpenCL Integration Methodology for FPGA Designs
Topi Leppänen[1], Panagiotis Mousouliotis[2], Georgios Keramidas[2], Joonas Multanen[1], Pekka Jääskeläinen[1]
1) Tampere University, Finland; 2) University of the Peloponnese, Greece

14:00 Accelerator Interface for Patmos
Clemens Lukas Pircher[1], Alexander Baranyai[1], Christoph Lehr[1], Martin Schoeberl[2]
1) Institute of Computer Engineering, TU Wien; 2) Department of Applied Mathematics and Computer Science, Technical University of Denmark

14:20 *Break*

15:00 *Parallel sessions*

Session: RF Circuits and Oscillators (Chair: Ted Johansson, Uppsala Univ., SE)

15:00 Low Power CMOS Thyristor-Based Relaxation Oscillator with Efficient Current Compensation
Marcel Jotschke[1], Gokulkumar Palanisamy[2], Wilmar Carvajal Ossa[1], Harsha Prabakaran[1], Jeongwook Koh[1], Matthias Kuhl[2], Wolfgang H. Krautschneider[2], Torsten Reich[1], Christian Mayr[3]
1) Fraunhofer EAS/IIS, Germany; 2) TU Hamburg, Germany; 3) TU Dresden, Germany

15:20 An LO Frequency Tripler with Phase Shifter and Detector in 28nm FD-SOI CMOS for 28-GHz Transceivers
Rikard Gannedahl, Henrik Sjöland
Lund University, Sweden

15:40 Broadband Analog Predistortion Circuits Utilizing Derivative Superposition
Sauli Haukka, Jere Rusanen, Alok Sethi, Aarno Pärssinen, Timo Rahkonen, Janne P. Aikio;
University of Oulu, Finland

Session: Digital Design and Verification (Chair: Snorre Aunet, NTNU, NO)

15:00 Clock Tree Generation by Abutment in Synchoros VLSI Design
Dimitrios Stathis, Panagiotis Chaourani, Syed M. A. H. Jafri, Ahmed Hemani
KTH Royal Institute of Technology, Sweden

15:20 RTL Delay Prediction using Neural Networks
Daniela Sánchez Lopera[1,2], Lorenzo Servadei[1], Priyanka Kasi Vishwa[1,2], Sebastian Siegfried Prebeck[1,2], Wolfgang Ecker[1,2]
1) Infineon Technologies AG, Germany; 2) Technical University of Munich, Germany

15:40 A Methodology for Automated Mining of Compact and Accurate Assertion Sets
Mohammad Reza Heidari Iman, Jaan Raik, Maksim Jenihhin, Gert Jervan, Tara Ghasempouri;
Tallinn University of Technology, Estonia

16:00 *Break*

16:20 **Plenary Session** (Chairs: Jari Nurmi, TAU, FI and Dag T. Wisland, Univ. Oslo, NO)

(Best Paper Award Candidates)

16:20 ChiselVerify: An Open-Source Hardware Verification Library for Chisel and Scala
Andrew Dobis[1], Tjark Petersen[1], Hans Jakob Damsgaard[1], Kasper Juul Hesse Rasmussen[1], Enrico Tolotto[1], Simon Thye Andersen[1], Richard Lin[2], Martin Schoeberl[1]
1) Technical University of Denmark, Denmark;
2) University of California - Berkeley, CA, USA

16:40 Approximate Computation on Commodity Computers through Bit-Serial Processing
Chuanjun Zhang, Shivangi Katiyar, Mitch Diamond, Olivier Franza
Intel Corporation, Massachusetts, USA

17:00 A 25.6-27.5GHz Phase-Locked Loop for SerDes Transceiver Clocking in 5nm FinFET
Ping Lu; Microsoft Corporate, USA

17:20 Keynote 2 (Chair: Kari Halonen, Aalto University, FI)
Mohammed Ismail, Wayne State University, US
Compact RF CMOS Radios for Emerging 5G/6G Wireless

18:20 *End of Day 1*

Wednesday Oct. 27

12:00 Keynote 3 (Chair: Jari Nurmi, TAU, FI)
Nele Mentens, Leiden University, the Netherlands, and KU Leuven, Belgium
Cybersecurity in Flexible Electronics

13:00 *Parallel sessions*

Special Session: Ultra-Low Voltage I (Chair: Orazio Aiello, NTU, SG)

13:00 An architecture for ultra-low-voltage ultra-low-power compressed sensing-based acquisition systems
Carmine Paolino[1], Fabio Pareschi[1,2], Mauro Mangia[3,2], Riccardo Rovatti[3,2], Gianluca Setti[1,2]
1) DET - Politecnico di Torino, Italy; 2) ARCES - University of Bologna, Italy; 3) DEI - University of Bologna, Italy

13:20 Low-Voltage Energy Efficient Neural Inference by Leveraging Fault Detection Techniques
Mehdi Safarpour[1], Mohammad Sabokrou[2], Tommy Zhongmin Deng[3], John Massingham[3], Lei Xun[4], Olli Silven[1]
1) Center for Machine Vision and Signal Analysis, University of Oulu, Finland;
2) Institute for Research in Fundamental Sciences (IPM), Tehran, Iran;
3) Huawei Technologies Sweden AB, Stockholm, Sweden;
4) University of Southampton, Southampton, UK

13:40 Bridging the gap between design and simulation of low voltage CMOS circuits
Cristina Missel Adornes, Deni Germano Alves Neto, Márcio Cherem Schneider, Carlos Galup-Montoro; Federal University of Santa Catarina, Brazil

Session: Wearable and Implantable Applications
(Chair: Ibraheem Shayea, Istanbul Technical University, TR)

13:00 Design of Low Power VLSI Architecture for Classification of Arrhythmic Beats Using DNN for Wearable Device Applications
Meenali Janveja, Mayank Tantuway, Ketan Chaudhari, Gaurav Trivedi
IIT Guwahati, India

13:20 Approximate Feature Extraction for Low Power Epileptic Seizure Prediction in Wearable Devices
Zain Taufique[1], Anil Kanduri[1], Muhammad Awais Bin Altaf[2], Pasi Liljeberg[1]
1) University of Turku, Finland;
2) Lahore University of Management and Sciences, Pakistan

13:40 Low-Complexity Unidimensional CNN based Brain Speller for Embedded Platforms
Giovanni Mezzina, Daniela De Venuto
Politecnico di Bari, Italy

14:00 *Break*

14:40 *Parallel sessions*

Special Session: Ultra-Low Voltage II (Chair: Orazio Aiello, NTU, SG)

14:40 Subthreshold Power PC and Nand Race free Flip-Flops in Frequency Divider Applications
Somayeh Hossein Zadeh, Snorre Aunet, Trond Ytterdal; NTNU, Norway

15:00 CMOS inverter linearization technique with active source degeneration

Luis Henrique Rodovalho[1], Cesar Ramos Rodrigues[1], Orazio Aiello[2]
1) Federal University of Santa Catarina, Brazil;
2) National University of Singapore, Singapore

15:20 *End of session*

Session: Signal Integrity (Chair: Martinez Alonso Abdel, Techidea, JP)

14:40 Signal Integrity in High Speed 3D IC Design- A Case Study

Shadi Harb[1], William Eisenstadt[2]
1) Intel Corporation, USA;
2) University of Florida, Electrical and Computer Engineering Dept, USA

15:00 Powerline Communication System-on-Chip in 180 nm Harsh Environment SOI Technology

Tobias Stuckenberg[1], Malte Rücker[2], Niklas Rother[1], Rochus Nowosielski[2], Frank Wiese[2], Holger Blume[1]
1) Institute of Microelectronic Systems, Leibniz Universitaet Hannover, Germany;
2) Drilling Services, Baker Hughes, Celle, Germany

15:20 A digital switching scheme to reduce DAC glitches using code-dependent randomization

Oscar Andres Morales[1], J Jacob Wikner[1], Liter Siek[2], Atila Alvandpour[1]
1) Linköping University, Sweden;
2) Nanyang Technological University, Singapore

15:40 *Break*

16:00 *Parallel sessions*

Session: Mixed-mode Design (Chair: Yong Chen (Nick), Univ. of Macao, MO)

16:00 Analysis and Design of Start-up Circuits for a 48V-12V Switched-Capacitor Converter in a 180nm SOI Process

Markus Mogensen Henriksen[1], Dennis Øland Larsen[2], Pere Llimós Muntal[1,2]
1) Technical University of Denmark, Kgs. Lyngby Denmark;
2) Skycore Semiconductors, Copenhagen Denmark

16:20 A Gate Voltage Sensing Ripple Reduction Control Technique for Switched-Capacitor DC-DC Converters

Christian Westmark Sønnichsen[1,2], Paul Stephansson[2]
1) Dept of Electrical Engineering, Technical University of Denmark, Denmark;
2) R&D Hardware Platforms IC, GN Hearing A/S, Ballerup, Denmark

16:40 Linearity Boosting Technique with Adaptive Sampling Switch Assisted by Signal Prediction for Multi-Channel ADCs in Standard CMOS Process

Zihao Jiao, Xiaofei Wang, Hongrui Luo, Jie Zhang, Ruizhi Zhang, Hong Zhang
Xi'an Jiaotong University, China

Special Session: Neural Network Implementations
(Chairs: Masoumeh Ebrahimi, KTH, SE and Kun-Chih (Jimmy) Chen, National Sun Yat-sen University, TW)

16:00 LOCAL: Low-Complex Mapping Algorithm for Spatial DNN Accelerators

Midia Reshadi, David Gregg; Lero, Trinity College Dublin, Ireland

16:20 Machine Learning Approach for Accelerating Simulation-based Fault Injection

Li Lu[1], Junchao Chen[1], Anselm Breitenreiter[1], Oliver Shrape[1], Markus Ulbricht[1], Milos Krstic[1,2]

1) IHP-Leibniz-Institut für innovative Mikroelektronik, Germany;
2) University of Potsdam, Germany

16:40 Intelligent Cognitive Radio Architecture Applying Machine Learning and Reconfigurability

Jari Nurmi[1], Darshika G. Perera[2]

1) Tampere University, Finland; 2) University of Colorado Colorado Springs, USA

17:00 *Break*

17:20 Keynote 4 (Chair: Jari Nurmi, TAU, FI)

Darshika G. Perera, University of Colorado Colorado Springs, USA

Reconfigurable Hardware Architectures for Edge Computing

18:20 **Awards and Closing** (Chair: Jari Nurmi, TAU, FI)

18:30 *End of NorCAS 2021*